

CLAIMS

What is claimed is:

- 1 1. In a processor adapted to cooperate with a coprocessor coupled
2 thereto via a communication bus in an execution of at least one
3 instruction comprising a count field and a code field, a method for
4 executing said instruction comprising the steps of:
5 receiving said instruction;
6 providing to said coprocessor, via a first cycle on said
7 communication bus, said count and code fields;
8 if the count field has a value, n, greater than zero, providing to
9 the coprocessor, via a second cycle on said communication
10 bus, a first operand; and
11 completing said instruction.
- 1 2. The method of claim 1 wherein said instruction has a mnemonic of
2 H_CALL.
- 1 3. The method of claim 1 further comprising the steps of:
2 receiving a first input signal from the coprocessor via said
3 communication bus during said first cycle.
- 1 4. The method of claim 3 wherein, if the first input signal received
2 from the coprocessor via the communication bus during said first
3 cycle has a first state, then repeating said first cycle, wherein the step
4 of repeating said first cycle includes:
5 providing to said coprocessor, via said first cycle on said
6 communication bus, said count and code fields; and
7 receiving said first input signal from the coprocessor via said
8 communication bus during said first cycle.
- 1 5. The method of claim 4 wherein, if the first input signal received
2 from the coprocessor via the communication bus during said first
3 cycle has a second state, then providing to said coprocessor, via said
4 second cycle on said communication bus, a first output signal.

1 6. The method of claim 5 further characterized in that the first output
2 signal is selectively provided to the coprocessor via said second cycle
3 on said communication bus.

1 7. The method of claim 4 further comprising the steps of:
2 if a count field value, n , is greater than one, then, on each of
3 $(n-1)$ cycles on said communication bus:
4 providing to the coprocessor, via said communication bus,
5 a next one of $(n-1)$ operands; and
6 receiving from the coprocessor, via said communication
7 bus, a second input signal.

1 8. The method of claim 7 wherein, if the second input signal received
2 from the coprocessor via the communication bus during a cycle, m ,
3 of said $(n-1)$ cycles, has a first state, then repeating said cycle m ,
4 wherein said step of repeating said cycle m includes:
5 providing to the coprocessor, via said communication bus, the
6 operand m ; and
7 receiving from the coprocessor, via said communication bus, said
8 second input signal.

1 9. The method of claim 1 further comprising the steps of:
2 if a count field value, n , is greater than one, then, on each of
3 $(n-1)$ cycles on said communication bus:
4 providing to the coprocessor, via said communication bus,
5 a next one of $(n-1)$ operands; and
6 receiving from the coprocessor, via said communication
7 bus, a second input signal.

1 10. The method of claim 9 wherein, if the second input signal received
2 from the coprocessor via the communication bus during a cycle, m,
3 of said (n-1) cycles, has a first state, then repeating said cycle m,
4 wherein said step of repeating said cycle m includes:
5 providing to the coprocessor, via said communication bus, the
6 operand m; and
7 receiving from the coprocessor, via said communication bus, said
8 second input signal.

1 11. The method of claim 1 wherein the processor is adapted to cooperate
2 with a plurality of coprocessors coupled thereto via said
3 communication bus in the execution of said instruction, the method
4 further comprising the step of:
5 providing to said plurality of coprocessors, via said
6 communication bus during said first cycle, an identifier field
7 having a value which uniquely identifies a selected one of said
8 plurality of coprocessors.

1 12. The method of claim 1 wherein the processor includes a plurality of
2 registers for storing selected operands, and wherein the step of
3 providing said first operand to said coprocessor via said
4 communication bus during said second cycle is further characterized
5 as:
6 if the count field has a value, n, greater than zero, providing to
7 the coprocessor, via a second cycle on said communication
8 bus, an operand stored in a predetermined one of said plurality
9 of registers.

1 13. The method of claim 1 further including the step of:
2 providing to the coprocessor, during at least a portion of said
3 second cycle on said communication bus, a second output
4 signal.

- 1 14. In a processor adapted to cooperate with a coprocessor coupled
2 thereto via a communication bus in an execution of at least one
3 instruction comprising an effective address calculation field, a
4 method for executing said instruction comprising the steps of:
5 receiving said instruction;
6 providing to said coprocessor, via a first cycle on said
7 communication bus, said effective address calculation field;
8 calculating an effective address in accordance with said effective
9 address calculation field;
10 fetching an operand stored at said calculated effective address;
11 providing to the coprocessor, via a second cycle on said
12 communication bus, said fetched operand; and
13 completing said instruction.
- 1 15. The method of claim 14 wherein said instruction has a mnemonic of
2 H_LD.
- 1 16. The method of claim 14 further comprising the steps of:
2 receiving a first input signal from the coprocessor via said
3 communication bus during said first cycle.
- 1 17. The method of claim 16 wherein, if the first input signal received
2 from the coprocessor via the communication bus during said first
3 cycle has a first state, then repeating said first cycle, wherein the step
4 of repeating said first cycle includes:
5 providing to said coprocessor, via said first cycle on said
6 communication bus, said effective address calculation field;
7 and
8 receiving said first input signal from the coprocessor via said
9 communication bus during said first cycle.
- 1 18. The method of claim 16 wherein, if the first input signal received
2 from the coprocessor via the communication bus during said first
3 cycle has a second state, then providing to said coprocessor, via said
4 second cycle on said communication bus, a first output signal.

1 19. The method of claim 18 further characterized in that the first output
2 signal is selectively provided to the coprocessor via said second cycle
3 on said communication bus.

1 20. The method of claim 14 further including the step of:
2 providing to the coprocessor, during at least a portion of said
3 second cycle on said communication bus, a first output signal.

1 21. The method of claim 14 wherein the processor includes a plurality of
2 registers for storing selected operands, wherein the effective address
3 calculation field comprises a base register designator subfield and a
4 displacement subfield, and wherein the step of calculating said
5 effective address in accordance with said effective address calculation
6 field includes adding the contents of said displacement subfield to the
7 contents of the one of said plurality of registers designated by the
8 contents of said base register designator subfield.

1 22. The method of claim 21 wherein the effective address calculation
2 field includes an update field and wherein the step of calculating said
3 effective address in accordance with said effective address calculation
4 field includes storing said calculated effective address in said
5 designated one of said plurality of registers if said update field has a
6 first value.

1 23. In a processor adapted to cooperate with a coprocessor coupled
2 thereto via a communication bus in an execution of at least one
3 instruction comprising an effective address calculation field, a
4 method for executing said instruction comprising the steps of:
5 receiving said instruction;
6 providing to said coprocessor, via a first cycle on said
7 communication bus, said effective address calculation field;
8 calculating an effective address in accordance with said effective
9 address calculation field;
10 receiving from the coprocessor, via a second cycle on said
11 communication bus, an operand;
12 storing said received operand at said calculated effective address;
13 and
14 completing said instruction.

1 24. The method of claim 23 wherein said instruction has a mnemonic of
2 H_ST.

1 25. The method of claim 23 further comprising the steps of:
2 receiving a first input signal from the coprocessor via said
3 communication bus during said first cycle.

1 26. The method of claim 25 wherein, if the first input signal received
2 from the coprocessor via the communication bus during said first
3 cycle has a first state, then repeating said first cycle, wherein the step
4 of repeating said first cycle includes:
5 providing to said coprocessor, via said first cycle on said
6 communication bus, said effective address calculation field;
7 and
8 receiving said first input signal from the coprocessor via said
9 communication bus during said first cycle.

1 27. The method of claim 25 wherein, if the first input signal received
2 from the coprocessor via the communication bus during said first
3 cycle has a second state, then providing to said coprocessor, via said
4 second cycle on said communication bus, a first output signal.

1 28. The method of claim 27 further characterized in that the first output
2 signal is selectively provided to the coprocessor via said second cycle
3 on said communication bus.

1 29. The method of claim 23 further including the step of:
2 receiving from the coprocessor, during at least a portion of said
3 second cycle on said communication bus, a second input signal.

1 30. The method of claim 23 further including the step of:
2 providing to the coprocessor, during at least a portion of a third
3 cycle on said communication bus, a first output signal.

1 31. The method of claim 23 wherein the processor includes a plurality of
2 registers for storing selected operands, wherein the effective address
3 calculation field comprises a base register designator subfield and a
4 displacement subfield, and wherein the step of calculating said
5 effective address in accordance with said effective address calculation
6 field includes adding the contents of said displacement subfield to the
7 contents of one of said plurality of registers designated by the
8 contents of said base register designator subfield.

1 32. The method of claim 31 wherein the effective address calculation
2 field includes an update field and wherein the step of calculating said
3 effective address in accordance with said effective address calculation
4 field includes storing said calculated effective address in said
5 designated one of said plurality of registers if said update field has a
6 first value.